DL5510

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10-Digit LCD Calculator With Punctuation

GENERAL DESCRIPTION

DL5510 is a CMOS LSI calculator chip with 10 digits arithmetic operations, single memory, extraction-of-square-root percentage calculation, auto power off and punctuation function,designed for FEM LCD operation with 1.5V power supply

APPLICATION

This specification contains complete information of functional operations,electrical characteristics, packaging, and crating requirements of DL5510

FUNCTIONS

- Four standard functions (+, -, x, +).
- Auto-constant calculations (constant : multiplicand, divisor, addend and subtrahend).
- Square and reciprocal calculations.
- Mark-up and mark-down calculations.
- Extraction of square root.
- Percentage calculations.
- Chain multiplication and division.
- Power calculations.
- Rough estimate calculations.
- Punctuation comma display.
- Clear key: ON/C, C,CE.

FEATURES

- Accumulating memory : M+, M-, RM, CM, RM/CM.
- Single chip CMOS construction.
- Floating decimal point.
- Overflow indication: E
- 10-digit LCD triplex.
- On-chip oscillator components.
- Very low power consumption.
- 1.5V bettery or solar cell power supply.
- Automatic power off feature.

FUNCTIONAL DESCRIPTION

a. **Floating point system**

i) 10 digits floating decimal point system, with leading zero suppression, Zero shift.

ii) Symbols : '-' negative number indicator.

: 'E' Error status indicator.

: 'M' Non-zero memory indicator.

: '**9**' punctuation comma

b. **Error Detections**

i) System errors occur when :

- The integral part of any calculation result exceeds 10 digits.
- The integral part of any memory calculation result exceeds 10 digits.
- The integral part of any addend or subtrahend to memory exceed 10 digits.
- The integral part of a mark-up or mark-down calculation result exceeds 10 digits.
- The division by zero.
- The extraction of square root of a negative number.

ii) Rough estimate calculation error

- The integral part of the result of any standard functions, percentage, square root, reciprocal or power calculations result exceed 10 digits.

c. **Error Indication**

i) System error

'0' is indicated in the 1-digit position and 'E' in the sign indicator position.

ii)Rough estimate calculation error

The high-order 10 digits of a calculation result is indicated together with 'E'. The decimal point is indicated in the position corresponding to a calculation result times 10^{-10}, and no zero shift is performed.

d. **Error Release**

i) System error can be released by the ON/C or C key.

ii)ON/C or C key can release a rough estimate calculation error and clear calculation result at once.

CE key can release only a rough estimate calculation error("E" flag).

e. **Number Entry**

Numerical can be entered up to 10 digits, Numerical entries that equal to 11 digits or more will be ignored.

f. **Memory Protection**

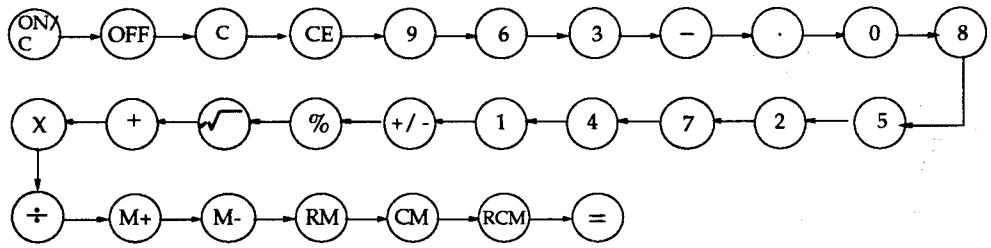
The memory contents present before any error detection are protected.

g. **Memory Indication**

If the memory content is non-zero, 'M' is indicated in the memory indicator position.

h. **Double Key Depression**

The order of priority when two keys are being depressed simultaneously is as follows :



i. **Key bounce protection**

i) Front edge : Minimum 3 words.

ii)Trailling edge : Minimum 16 words. (1 word is 3.3ms when display frequency is Fd=100Hz.)

j. **Auto Power Off**

Power automatically turns off after 5-6 minutes pass from the last key pressed.By connecting the APODIS pin to GND or V_{GG} , the auto power off function is disabled or enabled, respectively.

k. **Clear Operation**

All operations except memory contents are cleared by ON/C or C key.

l. **CE Key**

CE key can edit the last operand or operator.

ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Value	Unit	Note
Terminal voltage	V_{DD}	- 0.3 ~ + 2.1	V	1
	V_{IN}	- 0.3 ~ V_{DD} + 0.3		
Supply Voltage	V_{DD}	1.1~ 1.8	V	—
Operating temperature range	T_{OPR}	0 ~ + 50	° C	—
Storage temperature range	T_{STG}	- 55 ~ + 125	° C	—

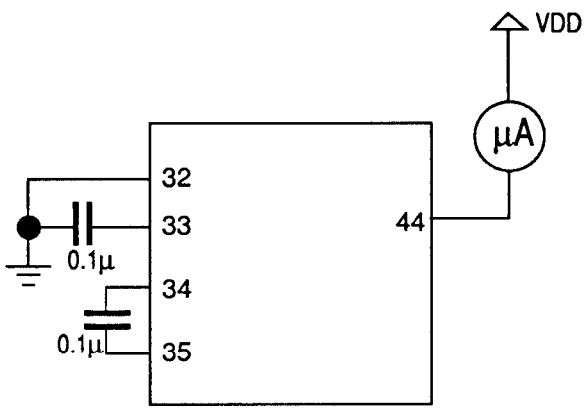
Note 1 : Maximum voltage on any pin is referenced to GND.

ELECTRICAL CHARACTERISTICS

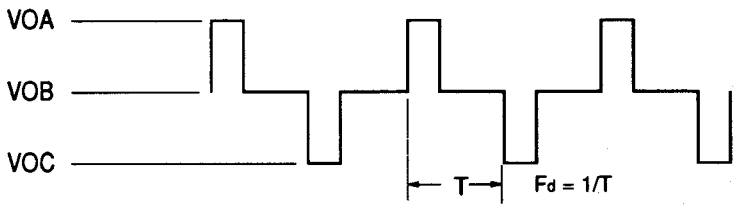
(Ta = 25°C, V_{DD} = 1.5V unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition	Note
Input Voltage 1	V_{IH1}	V_{DD}-0.4	—	—	V	—	2
	V_{IL1}	—	—	0.4		—	
Input Voltage 2	V_{IH2}	Vcc-0.8	—	—	V	Vcc=3v	3
	V_{IL2}	—	—	0.4		Vcc=3v	
Input Current 1	I_{IH1}	0.3	1	3	uA	Vin=0v,power off	2
	I_{IL1}	—	--	1		Vin=V_{DD}, power off	
Input Current 2	I_{IH2}	0.3	1	3	uA	Vin = 0v	3
	I_{IL2}	—	--	1		Vin = Vcc(3v)	
Output Voltage	V_{OA}	2.80	2.95	—	V	No load	4
	V_{OB}	1.30	1.50	1.70		No load	
	V_{OC}	—	0	0.20		No load	
Display Frequency	Fd	40	65	—	Hz	V_{DD} = 1.3V, while display is ON.	
Dissipation	I_{OFF}	--	--	0.1	µA	Display is OFF	5
	I_{DIS}	--	2	4		V_{DD} = 1.3V, without load	6
	I_{OP}	—	3	--		V_{DD} = 1.1V, without load	7

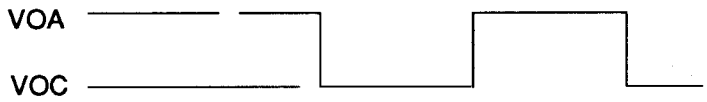
Note 2 : Applies to Pins FDIS, K2,TEST, EXT.
Note 3 : Applies to Pins K4 ~ K6 .
Note 4 : Applies to a1~a10, b1 ~ b10 ,c1~c10, H1~H3.
Note 5 : Measured by the bellow test circuit after power supply automatically turns off.
Note 6 : Measured by the bellow test circuit while "0" is being displayed after auto-clear operation and while no key is being depressed.
Note 7 : Measured by the bellow test circuit while operation is being made by ON/C key and while no key is being depressed.



LCD BACKPLANE OUTPUT WAVEFORM 1; HI (I=1,2,3)



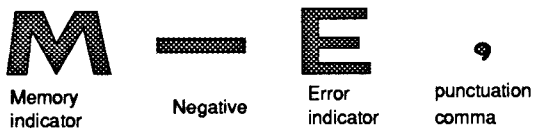
LCD BACKPLANE OUTPUT WAVEFORM 2; ai, bi, ci (i=1,2, - - - 10)



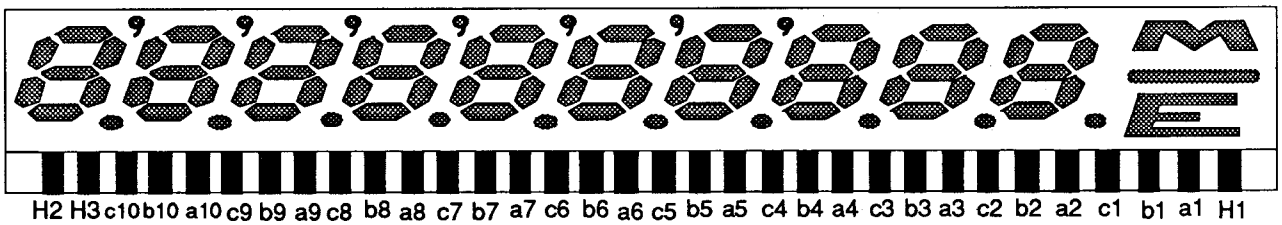
DISPLAY FONTS

a. **Numerical Font**

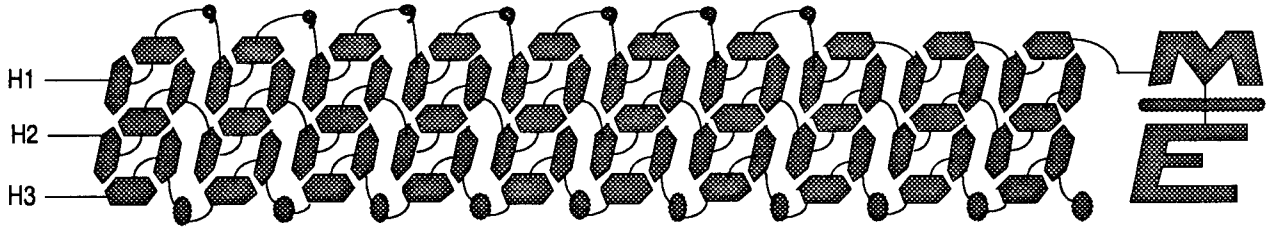
b. **Sign Font**



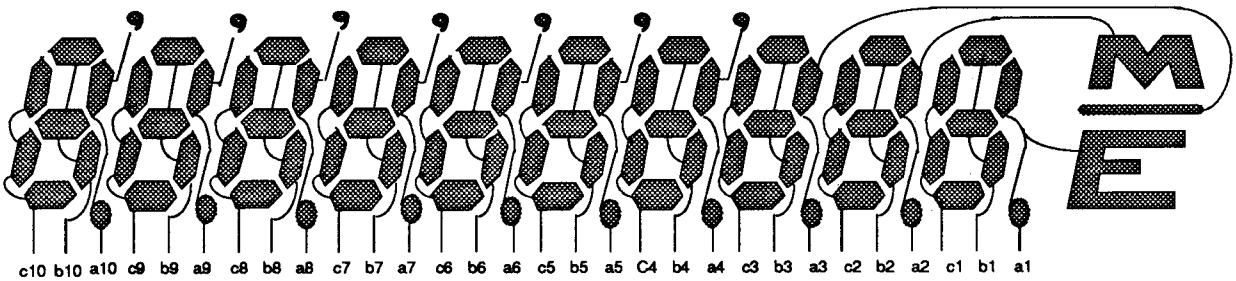
LCD CONNECTOR



LCD Panel



Backplanes Connection



Segment Connection

MARK-UP AND MARK-DOWN CALCULATION

Mark-up and mark-down calculation are performed as follows.

ENTRY		DISPLAY	
A + OR - B %	A X B % + OR - =	A A B A+AM/100 OR A-AM/100	A A B *AM/100 AM/100 A+AM/100 or A-AM/100

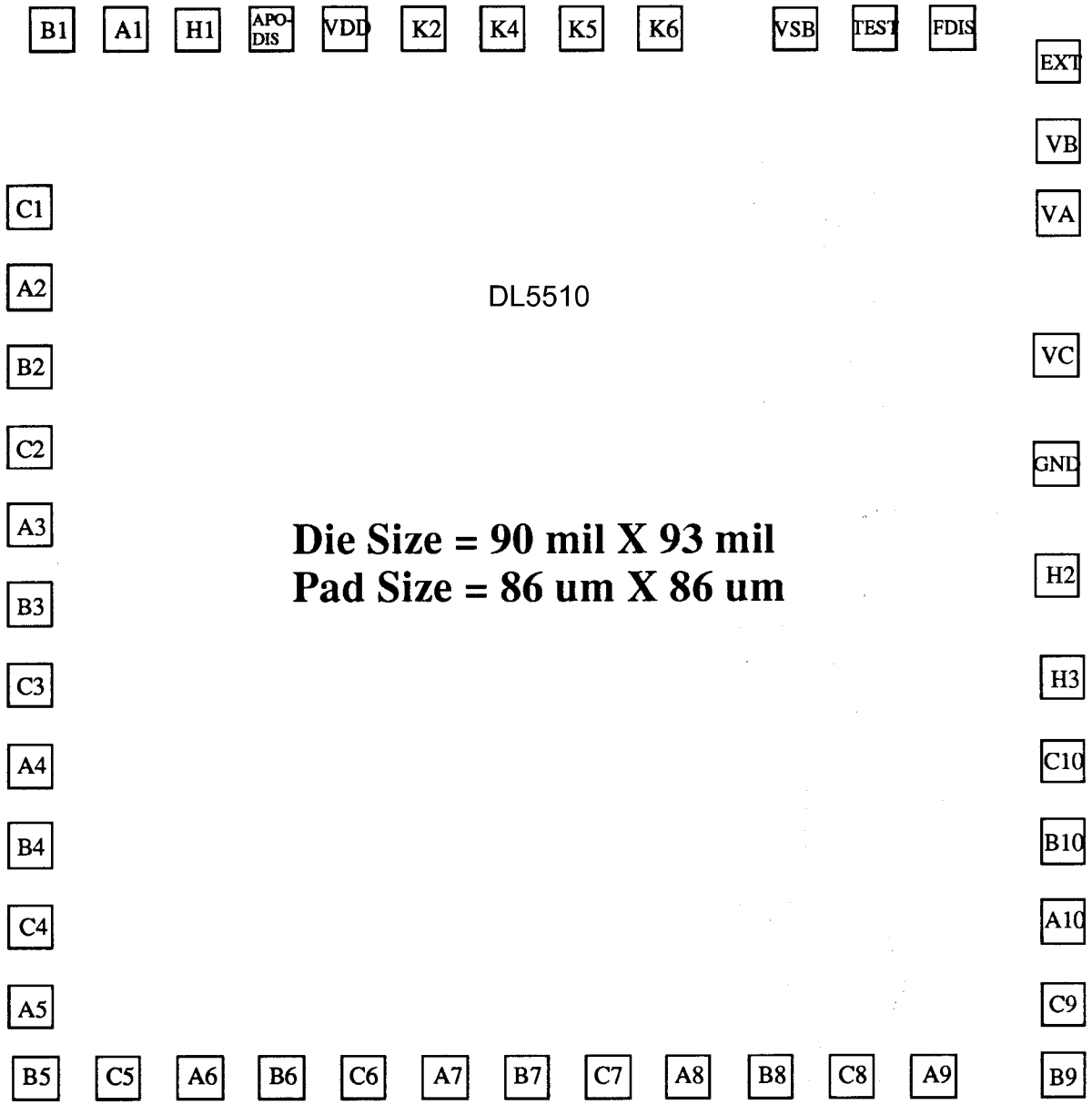
* AM : AMOUNT

PIN DESCRIPTIOON

Pin No.	Signal	I/O	Description
1	c1	O	Display output.
2	a2	O	Display output.
3	b2	O	Display output.
4	c2	O	Display output.
5	a3	O	Display output.
6	b3	O	Display output.
7	NC	-	No connection
8	c3	O	Display output.
9	a4	O	Display output.
10	b4	O	Display output.
11	c4	O	Display output.
12	a5	O	Display output.
13	b5	O	Display output.
14	c5	O	Display output.
15	a6	O	Display output.
16	b6	O	Display output.
17	c6	O	Display output.
18	a7	O	Display output.
19	b7	O	Display output.
20	c7	O	Display output.
21	a8	O	Display output /Strobe 9.
22	b8	O	Display output /Strobe 8.
23	c8	O	Display output /Strobe 7.
24	a9	O	Display output /Strobe 6.

Pin No.	Signal	I/O	Description
25	b9	O	Display output/Strobe 5.
26	c9	O	Display output/Strobe 4.
27	a10	O	Display output/Strobe 3.
28	b10	O	Display output/Strobe 2.
29	c10	O	Display output/Strobe 1.
30	H3	O	COMMON 3.
31	H2	O	COMMON 2.
32	GND		Ground.
33	VC	O	Capacitor pin for voltage set-up.
34	VA	O	Capacitor pin for voltage set-up.
35	VB	O	Capacitor pin for voltage set-up.
36	EXT	I	External clock.
37	FDIS	I	Fosc & frequency doubler disable
38	TEST	I	TEST pin.
39	VSB		Solar celll power supply
40	K6	I	Key input.
41	K5	I	Key input.
42	K4	I	Key input.
43	K2	I	Key input.
44	VDD		Power supply.
45	APODIS	I	Auto power off disable.
46	H1	O	COMMON 1.
47	a1	O	Display output.
48	b1	O	Display output.

PAD DIAGRAM



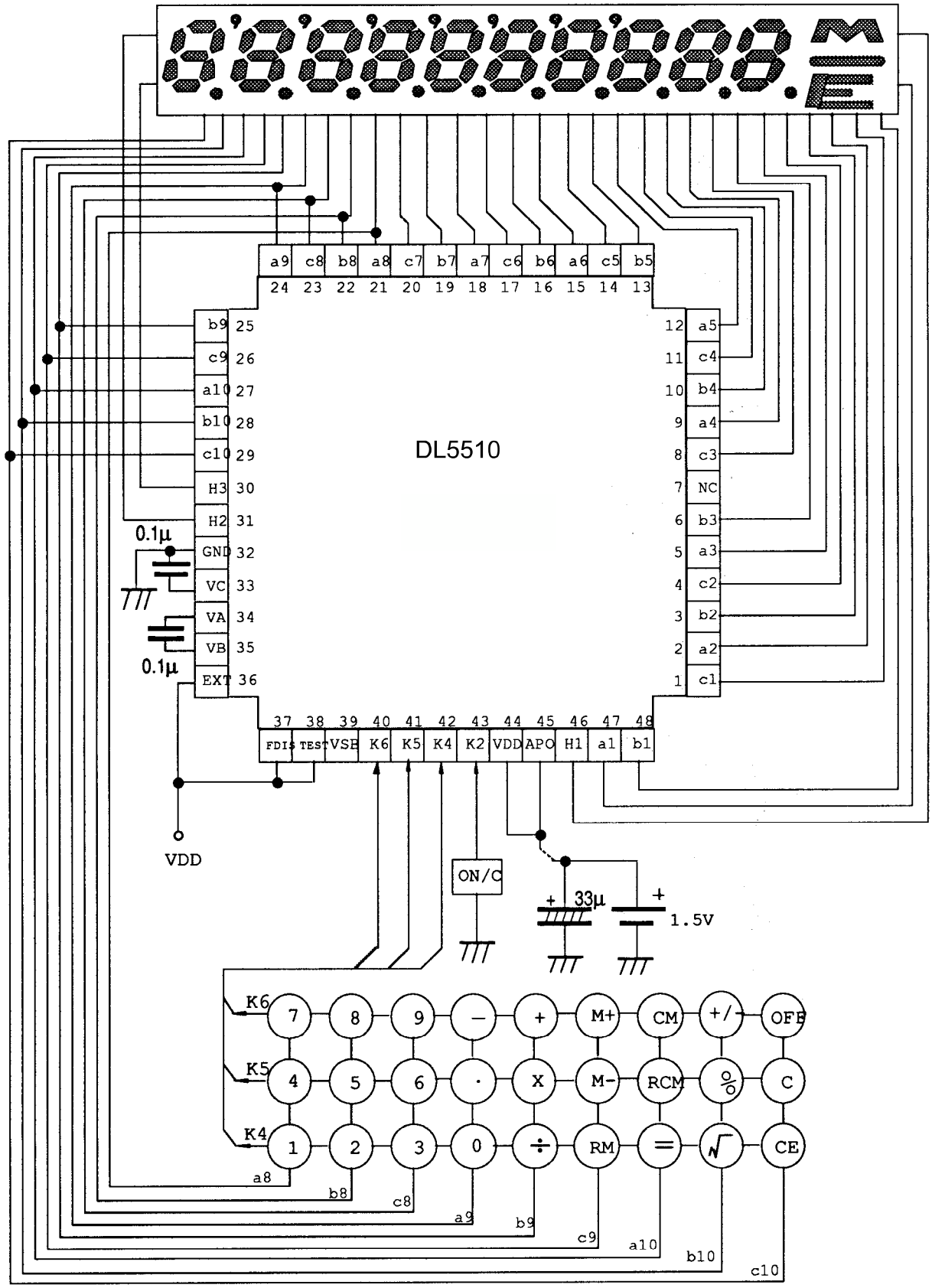
Die Size = 90 mil X 93 mil
Pad Size = 86 um X 86 um

The Co-ordinate for Low Left Corner of Each Pad

B5(-1043.9, -1086.1)	B9 (967.0, -1085.0)	FDIS (752.4, 1002.1)	C1(-1054.4, 651.6)
C5(-884.9, -1086.1)	C9 (968.4, -942.6)	TEST (599.6, 1002.1)	A2(-1054.4, 490.7)
A6(-724.0, -1086.1)	A10 (968.4, -779.8)	VSB (445.1, 1002.0)	B2(-1054.4, 333.4)
B6(-566.0, -1086.1)	B10 (968.4, -621.7)	K6 (179.3, 1002.1)	C2(-1054.4, 172.5)
C6(-404.5, -1086.1)	C10 (968.4, -460.8)	K5 (24.6, 1002.1)	A3(-1054.4, 14.4)
A7(-245.5, -1086.1)	H3 (968.4, -295.3)	K4 (-130.0, 1002.1)	B3(-1054.4, -146.5)
B7(-84.6, -1086.1)	H2 (957.6, -93.4)	K2 (-284.5, 1002.1)	C3(-1054.4, -305.3)
C7(74.2, -1086.1)	GND(955.4, 133.4)	VDD (-439.0, 1002.1)	A4(-1054.4, -466.2)
A8(231.9, -1086.1)	VC (955.4, 351.8)	APODIS(-581.6, 1002.1)	B4(-1054.4, -624.3)
B8(393.2, -1086.1)	VA (959.3, 634.9)	H1 (-724.9, 1001.3)	C4(-1054.4, -785.2)
C8(552.6, -1086.1)	VB (959.3, 776.6)	A1 (-866.9, 1002.1)	A5(-1054.4, -942.6)
A9(711.4, -1086.1)	EXT(960.2, 934.7)	B1 (-1008.9, 1002.1)	

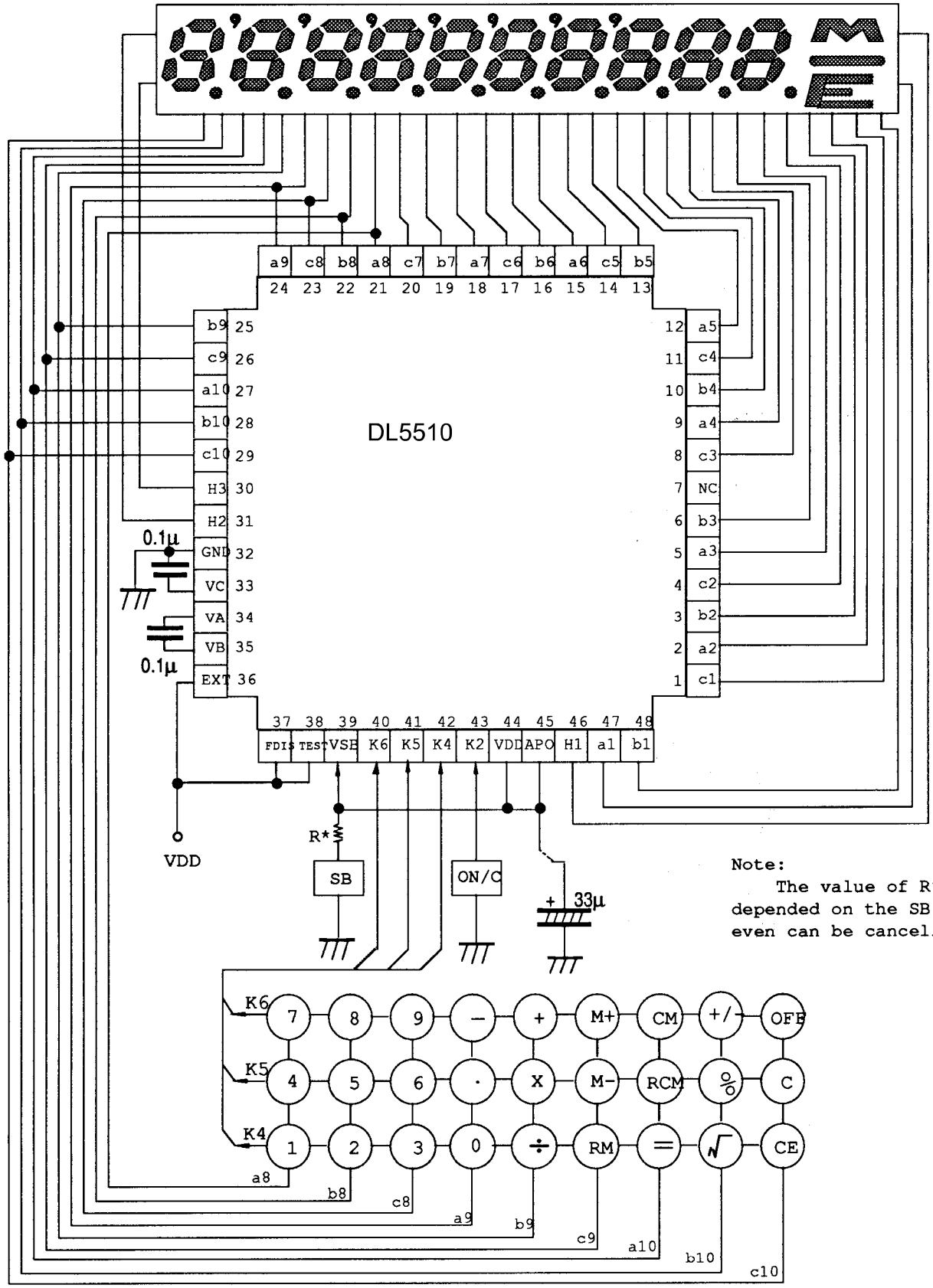
APPLICATION DIAGRAM FOR BATTERY SUPPLY

(Note: Chip substrate must be connected to GND or left floating)



APPLICATION DIAGRAM FOR SOLAR CELL SUPPLY

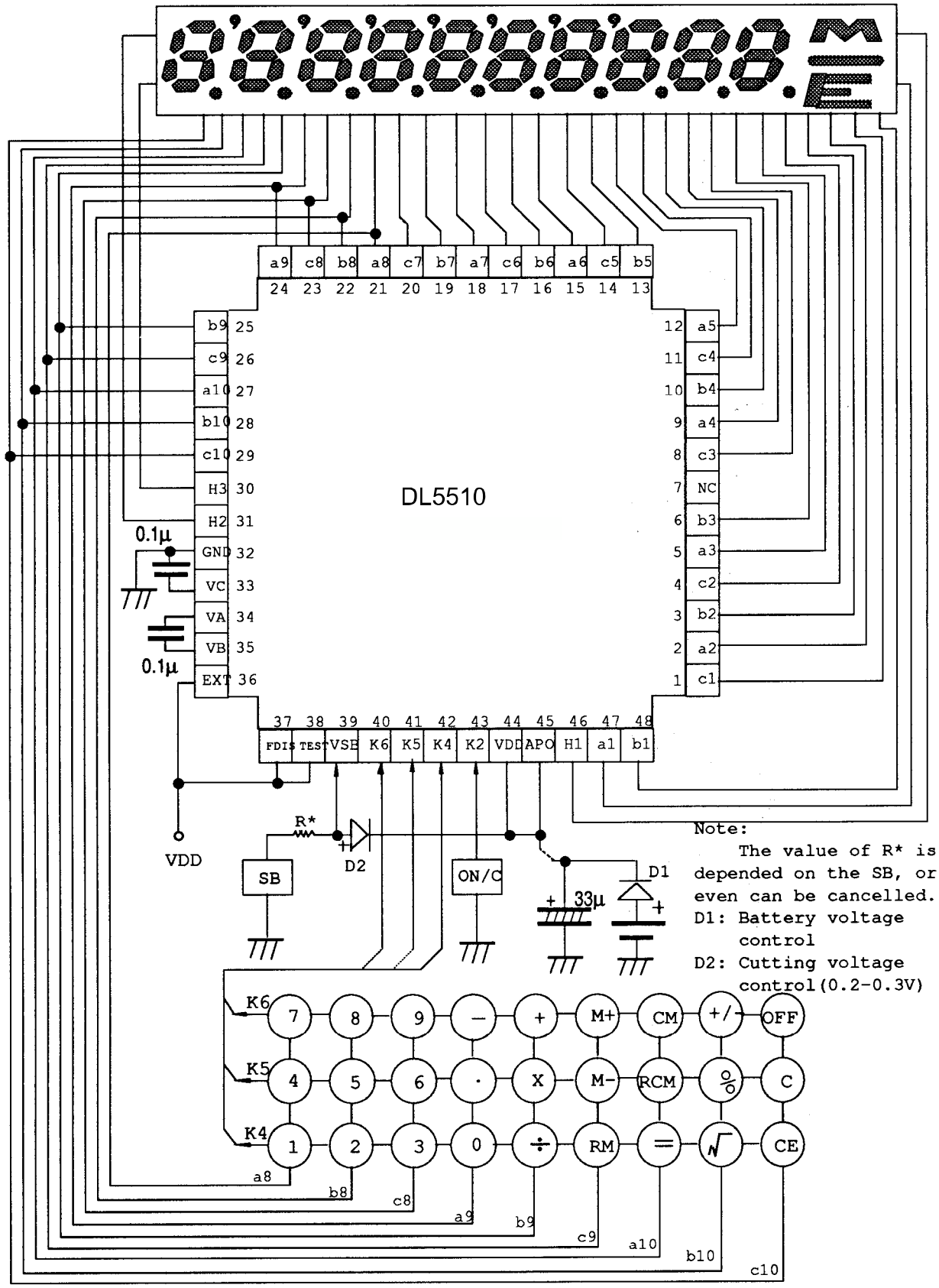
(Note: Chip substrate must be connected to GND or left floating)



Note:
The value of R* is depended on the SB, or even can be cancelled.

APPLICATION DIAGRAM For DUAL POWER SUPPLY

(Note: Chip substrate must be connected to GND or left floating)



Note:
The value of R* is depended on the SB, or even can be cancelled.
D1: Battery voltage control
D2: Cutting voltage control (0.2-0.3V)